Abstract of Disclosure

The claimed invention discloses an ESD protection circuit that is applied to an IC with power-down-mode operation. When the IC goes into power-down-mode operation, leakage current and charging from the I/O pad to the VDD power line could be prevented by applying the present invention. Therefore, the malfunction of the IC can be avoided. There still have two ESD clamp circuits respectively connected between the VDD power line and the VSS power line and between ESD bus line and VSS power line, so as to achieve the whole chip ESD protection scheme. The present invention can prevent ESD protection circuit from resulting in leakage current or malfunction under power-down-mode operation, and moreover achieve whole chip ESD protection scheme.